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10/805,593	03/19/2004	Jack B. Andersen	D2A1190-1	9249

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EXAMINER	
HUNG, STEPHEN C	

ART UNIT	PAPER NUMBER
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,593	ANDERSEN ET AL.	
	Examiner	Art Unit	
	Stephen C. Hung	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-19* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. **Claim 13** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The applicant is advised to show where the specification teaches transmitting "non-synchronization data to the slaves via the synchronization line."

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. **Claims 1, 3, 4, 6-10, 12, 14-16, and 18-19** are rejected under 35 U.S.C. 102(e) as being anticipated by **Moon et al. (US 6,799,234 B1)**.

Claim 1. Moon teaches a system (Figure 1) comprising:

a plurality of digital audio controller chips (Figure 1, master 10, slaves 12(1)-12(N))

a synchronization line (Figure 1, SYN) connected to each of the plurality of chips

wherein one of the plurality of chips is a master (Figure 1, master 10), and the remainder of the plurality of chips are slaves (Figure 1, slaves 12(1)-12(N))

wherein the master (Figure 1, master 10) is configured to generate a synchronization signal on the synchronization line (Figure 1, SYN)

wherein each of the slaves (Figure 1, slaves 12(1)-12(N)) is configured to detect the synchronization signal (Figure 1, SYN) and to begin synchronized operation in response to detecting the synchronization signal

Claim 3. Moon teaches the system of claim 1, wherein the master (Figure 1, master 10) is configured to detect the synchronization signal (Figure 1, SYN) and to begin synchronized operation in response to detecting the synchronization signal ("master device initiates an information transfer," column 1, lines 20-21)

Claim 4. Moon teaches the system of claim 1, wherein the master (Figure 1, master 10) is designated during an initialization process ("master device initiates an information transfer," column 1, lines 20-21)

Claim 6. Moon teaches the system of claim 1, wherein the synchronization signal (Figure 1, SYN) comprises a transition from a passive state ("switches 37 are closed," column 4, line 18) to an active state ("switch 37 are opened," column 4, line 26)

Claim 7. Moon teaches the system of claim 6, wherein the master (Figure 1, master 10) is configured to repeat the transition at a fixed intervals ("the master controls the number of fixed duration," column 3, line 1)

Claim 8. Moon teaches the system of claim 7, wherein the master (Figure 1, master 10) is configured to maintain the active state for a fixed period after each transition ("The master asserts the chip select but in the time slot assigned to the slave," column 4, lines 5-6)

Claim 9. Moon teaches the system of claim 8, wherein each slave is configured to sample the synchronization line during the fixed period to determine whether the synchronization line is in an active state ("the switch 37 is opened and the slave counters will once again beginning counting as described earlier," column 4, lines 26-27)

Claim 10. Moon teaches the system of claim 9, wherein each slave is configured to take multiple samples during the fixed period and to determine whether the synchronization line is in an active state based upon a majority of the multiple samples ("slave multiplexer control chip control logic 44 takes the reading of the RD 42, and begins monitoring the multiplexer bus's slave time slots," column 3, lines 57-60)

Claim 12. Moon teaches the system of claim 9, wherein each slave is configured to filter samples of the synchronization line ("slave multiplexer control chip control logic notes the next time slot, waits for one frame delay, and attempts to assert the assigned but of that slot," column 3, lines 65-67)

Claim 14. Moon teaches the system of claim 13, wherein the synchronization signal (Figure 1, SYN) comprises a transition from a passive state ("switches 37 are closed," column 4, line 18) to an active state ("switch 37 are opened," column 4, line 26), wherein the master (Figure 1, master 10) is configured to maintain the active state for a

fixed period ("fixed duration," column 3, line 1), then transition from the active state to the passive state, then maintain the passive state for a fixed period, then transmit data

Claim 15. Moon teaches the system of claim 1, wherein each of the slaves is configured to determine whether an error has occurred and, in response to detecting an error, to cause the master to re-synchronize the slaves ("If more than one slave selected the same assigned time slot, the master will detect the fact via a frame check sequence error on the SPU data. Having detected an error, the master issues a "reset" signal to that time slot in the next frame," column 4, lines 9-13)

Claim 16. Moon teaches the system of claim 15, wherein causing the master to re-synchronize comprises driving the synchronization line (Figure 1, SYN) to the active state (Figure 2, bit 0 = reset)

Claim 18. Moon teaches the system of claim 1, wherein the master (Figure 1, master 10) is configured to determine whether all of the slaves (Figure 1, slaves 12(1)-12(N)) are ready to begin synchronized operation before generating the synchronization signal ("a slave device is controlled by a master through a slave select line," column 1, lines 22-23)

Claim 19. Moon teaches the system of claim 18, wherein each of the slaves (Figure 1, slaves 12(1)-12(N)) is configured to drive the synchronization line (Figure 1, SYN) to an

active state ("switch 37 are opened," column 4, line 26) until the slave is ready to begin synchronized operation, and wherein the master is configured to determine that all of the slaves are ready to begin synchronized operation if the synchronization line is in a passive state ("switches 37 are closed," column 4, line 18)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Moon (US 6,799,234 B1)** in view of **Intrater et al. (5,822,779).**

Claim 2: Moon teaches digital audio controller chips. However, Moon does not teach that those chips are PWM chips.

In the same field of endeavor, Intrater teaches PWM chips (Figure 1, PWM 22).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to PWM chips, in a similar manner taught by Intrater, since a PWM chip

"generates a square wave with a fixed frequency and a variable duty cycle" (Intrater, column 2, lines 21-23).

5. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Moon (US 6,799,234 B1)** in view of **Burkhardt et al. (US 6,854,053 B2)**.

Claim 5: Moon teaches master and slaves chips. However, Moon does not teach that they have identical circuitry.

In the same field of endeavor, Burkhardt teaches master and slave chips with identical circuitry (Figure 1, master processor 12 and slave processor 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use identical circuitry, in a similar manner taught by Burkhardt, for the advantage of "identifying and communicating with each slave in a master-slave system in a simple and efficient manner" (Burkhardt, column 2, lines 63-65).

6. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Moon (US 6,799,234 B1)** in view of **Song (US 6,639,956 B1)**.

Claim 17. Moon teaches the system according to claim 1. However, Moon does not teach where the system is configured to align a phase of an output of each controller

chips by synchronizing the slaves with the master and to then stagger each of the phases.

In the same field of endeavor, Song teaches chips intended for the alignment of the phase difference ("phase detector 50 to align the local clock with the quarter clock," column 3, lines 42-43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to align the phase, in a similar manner taught by Song, since the phases "need to be in sync" (Song, column 1, line 40).

Allowable Subject Matter

7. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 7/03/2007 have been fully considered but they are not persuasive.

Consider **claim 1**, applicant argues that "These items are not digital audio controller chips" (page 5). However, Moon teaches that "the master is, for example, a network

control card and the slaves are stacked PC104+ cards." Although the PC104+ cards are general multi-purpose cards, the WinSystems PC104 Audio Module Datasheet teaches that "This module offers functionality industrial applications requiring audio, FM music synthesis, or sound effects enhancing." Thus, the PC104+ cards can be configured as digital audio controller chips.

The applicant further argues that "the Examiner incorrectly states that each of the slaves is configured to detect a synchronization signal on this line and to begin synchronized operation in response to detecting the signal." However, the time slots used on the synchronization line can be used as the synchronization signal. Moon states that "the master provides the multiplexing clock and frame sync" (column 3, lines 11-12) and "the slave multiplexer control chip control logic takes the reading of the RD and begins monitoring the multiplexer bus's slave time slots" (column 3, lines 58-61).

Furthermore, the synchronization signal is connected to all the slave chips to reduce time delays. Also, the reset signal can be used as a synchronization signal.

Consider **claim 3**, the applicant argues that "there is no indication that the master detects any signal or begins synchronize operation in response to such a detected signal" (page 6). However, Moon states that "the master detects the newly assigned slave time slot" (column 4, line 1-2).

Consider **claim 4**, applicant's arguments are non-persuasive for the same reasons in claim 3.

Consider **claim 6**, the applicant argues that "this portion of Moon clearly states that the opening and closing of switches is responsive to a reset signal detected during a selected time slot, and not in response to the synchronization signal" (page 6). However, the reset signal can be used as a synchronization signal.

Consider **claim 7**, the applicant argues that Moon fails to teach the claim limitation. However, the Moon reference controls a number of fixed time slots, therefore, it is transitioned at fixed intervals.

Consider **claim 8**. Moon teaches the system of claim 7, wherein the master (Figure 1, master 10) is configured to maintain the active state for a fixed period after each transition ("The master asserts the chip select but in the time slot assigned to the slave," column 4, lines 5-6)

Consider **claim 9**. Moon teaches the system of claim 8, wherein each slave is configured to sample the synchronization line during the fixed period to determine whether the synchronization line is in an active state ("the switch 37 is opened and the slave counters will once again beginning counting as described earlier," column 4, lines 26-27)

Consider **claim 10**. Moon teaches the system of claim 9, wherein each slave is configured to take multiple samples during the fixed period and to determine whether the synchronization line is in an active state based upon a majority of the multiple samples ("slave multiplexer control chip control logic 44 takes the reading of the RD 42, and begins monitoring the multiplexer bus's slave time slots," column 3, lines 57-60)

Consider **claim 12**. The applicant argues that "this has nothing to do with filtering the samples of the synchronization line" (page 7). However, if the slaves read information, then it is filtering samples of the synchronization line.

Applicant's arguments with respect to **claim 13** have been considered but are moot in view of the new ground(s) of rejection.

Consider **claims 14 and 15**. The applicant argues that Moon does not meet claim limitations. However, the reset signal can be used as a synchronization signal.

Consider **claim 16**. The applicant argues that "there is no disclosure whatsoever in Moon that the slaves can drive any signal on the synchronization line" (page 8). However, Moon states that "the master detects the newly assigned slave time slot" (column 4, lines 1-2).

Consider **claim 18**. The applicant argues that "this portion of Moon, however, only discloses that a master can control a slave through a slave select line- there is no suggestion whatsoever that the master determines the slaves are ready to begin synchronized operation before generating a synchronization signal" (page 8). However, Moon states that "the master detects the newly assigned slave time slot" (column 4, lines 1-2).

Consider **claim 19**, the applicant argues that "the slaves of Moon do not drive any signal on the synchronization line" (page 9). However, Moon states that "the master detects the newly assigned slave time slot" (column 4, lines 1-2).

Consider **claim 2**. The applicant argues that "neither Moon nor Intrater discloses audio controller chips" (page 9). However, Moon teaches that "the master is, for example, a network control card and the slaves are stacked PC104+ cards." Although the PC104+ cards are general multi-purpose cards, the WinSystems PC104 Audio Module Datasheet teaches that "This module offers functionality industrial applications requiring audio, FM music synthesis, or sound effects enhancing." Thus, the PC104+ cards can be configured as digital audio controller chips.

Applicant further argues that "the Examiner failed to show any motivation in the references or in the knowledge generally available to a person of ordinary skill in the art to combine the references" (page 9). However, Moon shows general purpose chips

which can be configured for different applications. Therefore, it would have been obvious to try the PWM chips of Intrater as the chips for Moon.

Consider **claim 5**, the applicant argues that "the master and slaves of Burkhardt therefore clearly do not have identical circuitry" (page 10). Consider Figure 1 of Burkhardt; although the physical location of the pull-up resistor resides in the master processor, the pull-up resistor is located on a common line 16, which is connected the each slave processor. Thus the pull-up resistor serves to supply power from the voltage supply to both master and slave processors. Thus, the master and slave processors have the same functions.

Consider **claim 17**, the applicant argues that "neither the Examiner nor Song suggest that the phases of the clock signals (or any other signals) should be staggered as recited in claim 17" (page 10). However, Song states that "Each of the three sampling clocks are configured to sample the incoming data and the quarter clock. A phase detector is also included to detect a phase difference between the quarter clock and the local clock" (abstract). Thus, the phases of the local and quarter clock in Song are staggered.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen C. Hung whose telephone number is (571)270-1457. The examiner can normally be reached on M-Th 7:30am-5pm, Every other Friday 7:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

S.H.

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